#### Notice of References Cited

Application/Control No.

10/695,606

Examiner

Stephen M. Baker

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#### **U.S. PATENT DOCUMENTS**

*	ł	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	Α	US-4,006,465	02-1977	Cross et al.	710/36
*	В	US-4,346,440	08-1982	Kyu et al.	709/236
*	С	US-4,357,703	11-1982	Van Brunt, Nicholas P.	714/733
*	D	US-4,366,478	12-1982	Masuda et al.	340/825
*	Е	US-4,468,733	08-1984	Oka et al.	710/312
*	F	US-4,482,999	11-1984	Janson et al.	370/452
*	G	US-4,488,259	12-1984	Mercy, Brian R.	714/726
*	Н	US-4,493,021	01-1985	Agrawal et al.	709/236
*	-	US-4,494,066	01-1985	Goel et al.	714/726
*	7	US-4,527,270	07-1985	Sweeton, David C.	714/47
*	ĸ	US-4,597,042	06-1986	d'Angeac et al.	714/730
*	L	US-4,638,313	01-1987	Sherwood et al.	340/825.52
*	М	US-4,680,733	07-1987	Duforestel et al.	377/64

#### **FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	0					
	Р					
	Ø					****
	R	-				
	S					
	Т					

#### **NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)				
	U	Avra, L., "A VHSIC ETM-Bus-Compatible Test and Maintenance Interface", IEEE International Test Conference, 1987, pp. 964-971				
	٧	Breuer, M. et al., "A Test and Maintenance Controller for a Module Containing Testable Chips", IEEE International Test Conference, 1988, pp. 502-513.				
	w	Whetsel, L., "A Standard Test Bus and Boundary Scan Architecture", TI Technical Journal, July-August 1988, pp. 48-59.				
	x	van Riessen, R., et al., "Design and Implementation of a Hierarchical Testable Architecture Using the Boundary Scan Technique", 1st European Test Conference, April 1989, pp. 112-118.				

<sup>\*</sup>A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

# Notice of References Cited

Application/Control No. 10/695,606	Applicant(s)/Pat Reexamination WHETSEL ET A		
Examiner	Art Unit		
Stephen M. Baker	2133	Page 2 of 3	

## U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	Α	US-4,694,293	09-1987	Sugiyama et al.	340/825.68
*	В	US-4,701,920	10-1987	Resnick et al.	714/733
*	С	US-4,710,933	12-1987	Powell et al.	714/730
*	D	US-4,748,617	05-1988	Drewlo, Kenneth G.	398/98
*	Е	US-4,768,190	08-1988	Giancarlo, Charles H.	370/400
*	F	US-4,791,358	12-1988	Sauerwald et al.	324/73.1
*	G	US-4,823,305	04-1989	Holdren et al.	710/30
*	Н	US-4,827,477	05-1989	Avaneas, Napoleon G.	714/757
*	1	US-4,860,000	08-1989	Kobayashi, Koji	340/825.5
*	J	US-4,866,421	09-1989	Szczepanek, Andre	340/825.52
*	К	US-4,866,508	09-1989	Eichelberger et al.	326/41
*	L	US-4,903,266	02-1990	Hack, George E.	714/719
*	М	US-4,931,722	06-1990	Stoica, Susana	714/733

#### **FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	0					
	P					
	Q					
	R					
	s					
	Т			,		

#### NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Lien, J-C, et al., "A Universal Test and Mainteance Controller for Modules and Boards", IEEE Transactions on Industrial Electronics, Vol. 36, No. 2, May 1989, pp. 231-240.
	V	No Author, "Test Bus Architecture", IBM Technical Disclosure Bulletin, Vol. 32, No. 3A, August 1989, pp. 21-27.
	w	LeBlanc, J., et al., "LOCST A Built-In Self-Test Technique", IEEE Design and Test, November 1984, pp. 45-52.
	x	Blair, J., et al., "A 16-Mbit/s Adapter Chip for the IBM Token-Ring Local Area Network", IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, December 1989, pp. 1647-1655.

A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

## Notice of References Cited

Application/Control No. 10/695,606	Applicant(s)/F Reexamination WHETSEL E	on
Examiner	Art Unit	
Stephen M. Baker	2133	Page 3 of 3

## U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	Α	US-4,944,038	07-1990	Hardy et al.	370/454
*	В	US-4,979,096	12-1990	Ueda et al.	709/248
*	С	US-5,051,985	09-1991	Cidon et al.	370/452
*	D	US-5,063,575	11-1991	Annamalai, Kadiresan	375/357
*	Е	US-5,247,626	09-1993	Firoozmand, Farzin	709/212
*	F	US-5,430,735	07-1995	Sauerwald et al.	714/731
*	G	US-5,657,329	08-1997	Sauerwald et al.	714/726
*	Н	US-5,687,179	11-1997	Whetsel et al.	714/726
*	ı	US-6,158,035	12-2000	Whetsel et al.	714/731
	J	US-			
	К	US-			
	L	US-			
	М	US-			

#### **FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	Z					
	0					
	Ρ					
	ď					
	R					
	Ø					
	Т					

#### **NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Wang, L-T., et al., "A Self-Test and Self-Diagnosis Architecture for Boards Using Boundary Scans", 1st European Test Conference, April 1989, pp. 119-126.
	V	
	w	
	х	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.